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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JIN YANG

Appeal 2008-005357
Application 09/608,637[1]
Technology Center 2100

Decided: July 21, 2009[2]

Before LEE E. BARRETT, JEAN R. HOMERE, and
JOHN A. JEFFERY, *Administrative Patent Judges*.

HOMERE, *Administrative Patent Judge*.

DECISION ON APPEAL

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[1] Filed on June 30, 2000. The real party in interest is Intel Corp.
[2] The two month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

STATEMENT OF THE CASE

Appellant appeals under 35 U.S.C. § 134(a) from the Examiner's non-final rejection of claims 4, 5, 8, 14 through 18, 28, and 31 through 40. Claims 1 through 3, 6, 7, 9 through 13, 19 through 27, 29, and 30 have been canceled. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm-in-part.

Appellant's Invention

Appellant invented a method and system for automatically verifying the design of a very large scale integrated (VLSI) circuit or other finite state systems. (Spec. 1: 5-7.) In particular, the invention relates to simulating a model of the VLSI circuit or other finite system (101), and subsequently verifying the behavior of the model against properties expressed in an assertion graph language. (Spec. 7: 12-14, 16: 18-21.) As depicted in Figure 3, upon computing a symbolic simulation relation for an assertion graph (102) on a first symbolic lattice domain (Figure 9), justification properties resulting therefrom are examined to verify the behavior of a corresponding circuit or the finite state system. (Spec. 30: 20 - Spec. 31: 24.)

Illustrative Claim

Independent claim 4 further illustrates the invention. It reads as follows:

4. A computer software product including one or more recordable media having executable instructions stored thereon which, when executed by a processing device, causes the processing device to perform, at least in part, a formal verification of a circuit or other finite-state system, said executable instructions causing the processing device to:

initialize a symbolic simulation relation for an assertion graph on a first symbolic lattice domain, wherein the assertion graph on the first symbolic lattice domain is configurable to express a justification property to verify by computing the symbolic simulation relation.

Rejections on Appeal

The Examiner rejects the claims on appeal as follows:

1. Claims 4, 5, 8, 14 through 18, 28, and 31 through 40 stand rejected under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Appellant regards as the invention.

2. Claims 4, 5, 8, 14 through 18, and 31 through 40 stand rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter.[3]

[3] Since the Examiner has withdrawn the § 101 rejection against independent claim 28, we presume that the same rejection is also withdrawn against claims 38 through 40 depending therefrom. (Ans. 5, 15.) We therefore will not address the non-statutory rejection against claims 28 and 38 through 40.

Appellant's Contentions

1. Appellant argues that the claim recitation of initializing a symbolic simulation relation in an assertion graph configured to express a justification property to verify by computing the symbolic simulation relation is not indefinite since it provides a linkage between circuit verification and initialization of a symbolic simulation relation for an assertion graph. (App. Br. 11.) In particular, Appellant argues that such linkage would be apparent to one of ordinary skill in the art in light of the Specification. (App. Br. 12-15.) Therefore, Appellant submits that the claim sets out and circumscribes with a reasonable degree of precision and particularity the cited limitation. (*Id.*)

2. Appellant argues that claims 4, 5, 8, 14 through 18, and 31 through 40 are directed to statutory subject matter. In particular, Appellant argues that since the computer software products of claims 4 and 8 are embodied on one or more recordable media, they thereby define structural and functional interrelationships between the computer program and with the rest of the computer to permit the computer's program to be realized. They are therefore directed to statutory subject matter. (App. Br. 20-21.) Further, Appellant argues that the methods of claims 14 and 16 are is directed to statutory subject matter since they recite a computer for executing the program instructions. (App. Br. 22-25.)

The Examiner's Findings/Conclusions

1. The Examiner avers that the claim language is disjoint since it fails to specify how the assertion graph is generated, and how the generated assertion graph relates to circuit design. (Ans. 4, 6.) The Examiner acknowledges that the Specification discusses various methods for generating the assertion graph (manual or automatic). (Ans. 7-9.) However, the Examiner finds that such disclosures cannot be read into the claim. Rather, the claims must be given their broadest reasonable interpretation. (Ans. 9-10.) Further, the Examiner finds that, given that two alternatives are discussed in the Specification for generating the assertion graph, the ordinarily skilled artisan would not be able to particularly ascertain which of the two disclosed methods to use in the circuit design. (Ans. 10-11.)

2. The Examiner submits that claims 4, 5, 8, 14 through 18, and 31 fail to pass muster under the tangible, concrete, and useful result test. In particular, the Examiner finds that the claims lack a useful result since the recitation of other finite state systems is not tied to the physical world. Therefore, these claims are directed to a mathematical construct that is an abstract idea. The Examiner thus finds the cited claims not to be directed to statutory subject matter under the cited test. (Ans. 3-4, 11-15.)

ISSUES

1. Has Appellant shown that the Examiner erred in finding that claims 4, 5, 8, 14 through 18, 28, and 31 through 40 are indefinite for failing to particularly point out and distinctly claim the subject matter which Appellant regards as the invention?

2. Has Appellant shown that the Examiner erred in finding that claims 4, 5, 8, 14 through 18, and 31 through 40 are directed to non-statutory subject matter?

PRINCIPLES OF LAW

1. Indefiniteness

The test for definiteness under 35 U.S.C. § 112, second paragraph, is whether "those skilled in the art would understand what is claimed when the claim is read in light of the specification." *Orthokinetics, Inc. v. Safety Travel Chairs, Inc.*, 806 F.2d 1565, 1576 (Fed. Cir. 1986).[4] The claim as a whole must be considered to determine whether it apprises one of ordinary skill in the art of its scope, and therefore serves the notice function required

[4] "The legal standard for definiteness is whether a claim reasonably apprises those of skill in the art of its scope." *In re Warmerdam*, 33 F.3d 1354, 1361 (Fed. Cir. 1994) (citing *Amgen Inc. v. Chugai Pharmaceutical Co. Ltd.*, 927 F.2d 1200, 1217 (Fed. Cir.1991)). The "inquiry therefore is merely to determine whether the claims do, in fact, set out and circumscribe a particular area with a reasonable degree of precision and particularity." *In re Moore*, 439 F.2d 1232, 1235 (CCPA 1971).

by 35 U.S.C. § 112, second paragraph by providing clear warning to others as to what constitutes the infringement of the patent. *Solomon v. Kimberly-Clark Corp.,* 216 F.3d 1372, 1379 (Fed. Cir. 2000.) If the language of the claim is such that a person of ordinary skill in the art could not interpret the metes and bounds of the claims so as to understand how to avoid infringement, a rejection of the claim under 35 U.S.C. § 112, second paragraph is deemed appropriate. *Morton Int'l, Inc. v. Cardinal Chemical Co.,* 5 F.3d 1464, 1470 (Fed. Cir. 1993).

2. Non-statutory Subject Matter

The Court of Appeals for the Federal Circuit has recently clarified the law regarding patent eligible subject matter for process claims. *In re Bilski,* 545 F.3d 943 (Fed. Cir. 2008) (en banc), *cert. granted*, No. 08-964, 2009 WL 221232 (U.S. June 1, 2009). The en banc court in *Bilski* held that "the machine-or-transformation test, properly applied, is the governing test for determining patent eligibility of a process under § 101." *Id.* at 956. The court in *Bilski* further held that "the 'useful, concrete and tangible result' inquiry is inadequate [to determine whether a claim is patent-eligible under § 101.]" *Id.* at 959-60. The court explained the machine-or-transformation test as follows:

> The machine-or-transformation test is a two-branched inquiry; an applicant may show that a process claim satisfies § 101 either by showing that his claim is tied to a particular machine, or by showing that his claim transforms an article. *See* [*Gottschalk v.*]*Benson,* 409

> U.S. [63] at 70, 93 S. Ct. 253 [(1972)]. Certain considerations are applicable to analysis under either branch. First, as illustrated by *Benson* and discussed below, the use of a specific machine or transformation of an article must impose meaningful limits on the claim's scope to impart patent-eligibility. *See Benson,* 409 U.S. at 71-72, 93 S. Ct. 253. Second, the involvement of the machine or transformation in the claimed process must not merely be insignificant extra-solution activity. *See* [*Parker v.*]*Flook,* 437 U.S. [584] at 590, 98 S. Ct. 2522 [(1978)].

Id. at 961-62.

The court declined to decide under the machine implementation branch of the inquiry whether or when recitation of a computer suffices to tie a process claim to a particular machine. As to the transformation branch of the inquiry, however, the court explained that transformation of a particular article into a different state or thing "must be central to the purpose of the claimed process." *Id.* at 962. As to the meaning of "article," the court explained that a chemical or physical transformation of physical objects or substances is patent-eligible under § 101. *Id.* The court also explained that transformation of data is sufficient to render a process patent-eligible if the data represents physical and tangible objects, i.e., transformation of such raw data into a particular visual depiction of a physical object on a display. *Id.* at 963. The court further noted that transformation of data is insufficient to render a process patent-eligible if the data does not specify any particular type or nature of data and does not specify how or where the data was obtained or what the data represented. *Id.* at 962 (citing *In re Abele,* 684 F.2d 902, 909 (CCPA 1982) (process claim of graphically displaying

variances of data from average values is not patent-eligible) and *In re Meyer,* 688 F.2d 789, 792-93 (CCPA 1982) (process claim involving undefined "complex system" and indeterminate "factors" drawn from unspecified "testing" is not patent- eligible)).

ANALYSIS

Indefiniteness Rejection

Independent claim 4 recites in relevant part initializing a symbolic simulation for an assertion graph on a first symbolic lattice domain configurable to express a justification property to verify by computing the symbolic simulation relation. Appellant's Specification reveals that the assertion graph is a monitor of a circuit, which can change over time. Upon simulating the circuit, the results obtained therefrom are verified against the consequences in the assertion graph. (Spec. 16: 18-20.) We find that the cited textual portion of the Specification clearly establishes a link between the assertion graph and the circuit being simulated. One of ordinary skill in the art, having read the Specification, would readily recognize that the circuit is first rendered as an assertion graph, which is subsequently simulated to examine the consequences or behavior resulting therefrom. The Examiner's position with respect to the standard for definiteness is untenable. As set forth in the Principles of Law section, the determination of whether or not a claim is definite should be made within the context of Appellant's Specification, and not in a vacuum. In our view, the Examiner

confounds the acceptable practice of reviewing the claim language in light of the Specification with the impermissible practice of reading limitations from the Specification into the claim. Further, the Examiner's finding that the claim is indefinite because the Specification recites two alternatives for generating the claimed assertion graph suggests that the Examiner mistakes the breadth of the claim for indefiniteness of the same. We thus find that the ordinarily skilled artisan, having read Appellant's Specification, would be apprised of the scope of the claim. It follows that Appellant has shown that the Examiner erred in finding that claim 4 is indefinite.

We find that Appellant has also shown error in the Examiner's rejection of claims 5, 8, 14 through 18, 28, and 31 through 40 for the reasons discussed above.

Non-Statutory Rejection of Program Product Claims

Claim 4 recites in relevant part a program product including one or more recordable media having executable instructions stored thereon, when executed by a processing device, cause the processing device to perform the verification of a circuit or other finite state system. Appellant's Specification reveals that a computer system receives data structures and simulation relation programs stored or transmitted on removable storage devices. (Spec. 35: 5-18.) Because the claim is drawn to a computer program product tangibly embodied in a storage medium, we find that the claim is directed to an article of manufacture. We thus find that the claim is

directed to a statutory subject matter. It follows that Appellant has shown that the Examiner erred in finding that claim 4 are directed to non-statutory subject matter.

Because claims 5, 8, and 31 through 37 recite these same limitations, we find that Appellant has shown error in the Examiner's rejection of those claims for the reasons discussed above.

Non-Statutory Rejection of Method Claims

The preamble of independent claim 14 recites a computer-implemented method for performing a formal verification of a circuit or other finite state system. The body of the claim recites, *inter alia*, initializing a symbolic simulation relation for an assertion graph of a symbolic lattice domain to express a justification property to verify through computing the symbolic simulation relation. We find that the claimed method is not transforming a physical object into a different state or thing. *See Bilski*, 545 F.3d at 962. We find that the computation of the symbolic simulation relations of the assertion graph to be the manipulation of a pure mathematical construct. Next, we find that the claimed method is not tied to a particular machine for executing the claimed steps. We recognize that the claim recites a computer-implemented method[5] that verifies the justification

[5] The preamble of claim 4 includes only a nominal recitation of a "computer-implemented method." Nominal recitations of structure in an otherwise ineligible method fail to make the method a statutory process. *See Benson*, 409 U.S. at 71-72. As *In re Comiskey*, 499 F.3d 1365 (Fed. Cir. 2007),

properties of the symbolic simulation relations for an assertion graph. However, the recited computer is a general purpose computer, and not a particular machine. This recitation is so generic as to encompass any computing system, such that anyone who performed this method in practice would fall within the scope of these claims. As such, we fail to find that this recitation alone requires the claimed method to include a particular machine such that the method qualifies as a "process" under § 101. We will not allow such a nominal recitation in the preamble to convert an otherwise ineligible claim into an eligible one. *See Ex parte Langemyr*, 89 USPQ2d 1988, 1996 (BPAI 2008) (informative).

Therefore, under the cited test, the claim fails to recite a method that is directed to statutory subject matter.

We note that the various arguments that the claims are directed to statutory subject matter under the useful, concrete, and tangible result test are moot since the Court of Appeals for the Federal Circuit has cautioned us against using this test in evaluating method claims for patent eligibility. *Bilski*, 545 F.3d at 959-60. It follows that Appellant has failed to show that the Examiner erred in finding claim 14 unpatentable as being directed to non-statutory subject matter.

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recognized, "the mere use of the machine to collect data necessary for application of the mental process may not make the claim patentable subject matter." *Id.* at 1380 (citing *In re Grams*, 888 F.2d 835, 839-40 (Fed. Cir. 1989)).

Appellant argues claims 14 through 18 as a single group. In accordance with 37 C.F.R. § 41.37(c)(1)(vii), the cited claims stand or fall with independent claim 14.

CONCLUSIONS OF LAW

A. Appellant has shown that the Examiner erred in finding that:

1. claims 4, 5, 8, 14 through 18, 28, and 31 through 40 are unpatentable under 35 U.S.C. § 112, second paragraph as being indefinite.

2. claims 4, 5, 8, and 31 through 37 are unpatentable under 35 U.S.C. § 101 as being directed to non-statutory subject matter.

B. We reverse these rejections.

C. Appellant has not shown that the Examiner erred in finding that claims 14 through 18 are unpatentable under 35 U.S.C. § 101 as being directed to non-statutory subject matter.

D. We affirm this rejection.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

msc

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